What is claimed is:

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1. A semiconductor device comprising:

(a) a substrate having a surface;

(b) a dielectric formed over the surface of the substrate; and

(c) a wiring line buried in the first dielectric layer;

the wiring line including a Cu-based conductor and a first cover layer covering an outer surface of the conductor;

the first cover layer being made of refractory metal nitride.

2. The device according to claim 1, wherein the first cover layer is made of nitride of at least one selected from the group consisting of titanium (Ti), tantalum (Ta), and tungsten (W).

3. The device according to claim 1, further comprising a second cover layer provided between the conductor and the first cover layer;

wherein the second cover layer covers partially or entirely the outer surface of the conductor, the second cover layer being made of refractory metal.

4. The device according to claim 1, further comprising a third cover layer provided between the conductor and the first cover layer;

wherein the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric.

5. The device according to claim 4, wherein the third cover layer covers the outer surface of the conductor at its each side.

6. The device according to claim 1, further comprising a second cover layer provided between the conductor and the first cover layer and a third cover layer provided between the conductor and the first cover layer;

wherein the second cover layer covers partially or entirely the outer surface of the conductor, the second cover layer being made of refractory metal;

and wherein the third cover layer covers entirely or partially the outer surface of the conductor, the third cover layer being made of dielectric.

7. The device according to claim 1, wherein the dielectric formed over the surface of the substrate is made of inorganic material and has a relative dielectric constant ranging from 1.6 to 9.

8. The device according to claim 1, wherein the dielectric formed over the surface of the substrate is made of organic material and

has a relative dielectric constant of 1.6 to 3.

9. The device according to claim 1, wherein the wiring line has a damascene structure.

10. The device according to claim 1, wherein the dielectric in which the wiring line is buried has a composite structure comprising a first dielectric layer, an etch stop layer formed on the first dielectric layer, and a second dielectric layer formed on the etch stop layer;

and wherein the bottom of the first cover layer is approximately in a same level as an upper surface of the first dielectric layer;

and wherein the top of the first cover layer is approximately in a same level as an upper surface of the second dielectric layer.

11. The device according to claim 1, wherein the dielectric in which the trench has inner side faces tilted at an angle of 70° to 85° with respect to an imaginary plane of a bottom of the trench.

12. A method of fabricating a semiconductor device, comprising the steps of:

(a) forming a first dielectric layer over a surface of a

substrate;

(c) forming a trench in the first dielectric layer;

(d) covering an inner surface of the trench with a first nitride of refractory metal;

(e) forming a Cu-based conductor on the first nitride of refractory metal in the trench;

(f) covering a top surface of the conductor in the trench with a second nitride of refractory metal;

(g) polishing the first dielectric layer until a polished surface of the first dielectric layer is approximately in a same level as a surface of the second nitride of refractory metal that covers the top surface of the conductor in the trench; and

(h) forming a second dielectric layer on the polished surface of the first dielectric layer to cover the surface of the second nitride of refractory metal in the trench;

wherein the Cu-based conductor is entirely covered with the first nitride of refractory metal and the second nitride of refractory metal in the trench;

and wherein the Cu-based conductor, the first nitride of refractory metal, and the second nitride of refractory metal constitute a Cu-based wiring line.

13. The method according to claim 12, wherein the trench is formed to have inner side faces tilted an angle of 70° to 85° with respect

to an imaginary plane of a bottom of the trench in the step (c).

14. The method according to claim 12, wherein in the step (e) of forming the Cu-based conductor on the first nitride of refractory metal in the trench, part of the conductor is deposited by sputtering and then, the remaining conductor is deposited by plating.

15. The method according to claim 12, wherein in the step (e) of forming the Cu-based conductor, the conductor is formed in such a way that the conductor has a height less than a depth of the trench.

16. The method according to claim 12, wherein in the step (g) of polishing the first dielectric layer, a CMP process is used;

and wherein end detection of the CMP process is performed by detection of polishing of the first dielectric layer after unnecessary second nitride of refractory metal deposited on the first dielectric layer is completely removed.

17. The method according to claim 12, wherein in the step (d) of covering the inner surface of the trench, nitride of at least one selected from the group consisting of titanium (Ti), tantalum (Ta), and tungsten (W) is used as the first nitride of refractory metal.

18. The method according to claim 12, further comprising a step

of depositing a first refractory metal layer on the inner surface of the trench between the step (c) of forming the trench and the step (d) of covering the inner surface of the trench;

wherein the first nitride of refractory metal is deposited on the first refractory metal layer in the step (d);

and wherein the first refractory metal layer is used for forming a second cover layer that covers partially or entirely the Cu-based conductor.

19. The method according to claim 18, further comprising a step of depositing a second refractory metal layer on the top surface of the conductor between the step (e) of forming the Cu-based conductor and the step (f) of polishing the first dielectric layer;

wherein the second refractory metal layer is located on the top surface of the conductor in the trench;

and wherein the first and second refractory metal layers form the second cover layer that covers entirely the Cu-based conductor.

20. The method according to claim 12, further comprising a step of selectively depositing a dielectric on the first nitride of refractory metal in the trench is added between the step (d) of covering the top surface of the conductor and the step (e) of forming the Cu-based conductor;

wherein the dielectric thus deposited is located at each side of the Cu-based conductor in the trench to expose the bottom of the trench;

and wherein the dielectric is used for forming a third cover layer that covers partially or entirely the Cu-based conductor.

21. The method according to claim 20, wherein the step of selectively depositing the dielectric on the first nitride of refractory metal includes a sub-step of depositing the dielectric on the first nitride of refractory metal and a sub-step of selectively etching part of the dielectric at the bottom of the trench.

22. The method according to claim 12, wherein the first cover layer is made of nitride of at least one selected from the group consisting of titanium (Ti), tantalum (Ta), and tungsten (W).

23. The method according to claim 12, wherein the first dielectric layer formed over the surface of the substrate is made of inorganic material and has a relative dielectric constant ranging from 1.6 to 9.

24. The method according to claim 12, wherein the first dielectric layer is made of organic material and has a relative dielectric constant of 1.6 to 3.